DESIGN OF HIGH PERFORMANCES GILBERT-CELL MIXERS FOR GSM/DCS FRONT-ENDS

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Abstract

This paper reports an original design methodology for low voltage high performances Gilbert mixers in the DCS range. We present for the first time a real BiCMOS structure featuring +10.6 dB conversion gain, +6.7 dBm IP3, 10.3 DSB noise figure under a 2.2 V supply voltage, which is among the best results ever reported.

Introduction

The Gilbert-cell is the most widely used frequency mixer in RF front-ends. Its double-balanced structure offers spectral quality and intrinsic port-to-port isolation that match very well the GSM/DCS (and other standards) specifications [1]. But its four stages architecture is not well suited for lowering the supply voltage. This paper addresses an original methodology of Gilbert mixer design in the 1.8 GHz frequency range, providing high performances both in term of conversion gain, linearity, noise level and power consumption.

Section I presents a theoretical analysis of the Gilbert mixer. Section II is related to the design methodology employed to achieve the requirements through a conventional BJT and a real BiCMOS Gilbert mixer conceptions. The conclusions are outlined in section III.

Theoretical Analysis

In Gilbert mixers, the signal enters a RF differential transconductor pair (controlled by a DC current I_0), whose output currents are commutated by the switching behavior of a quad of LO devices, to perform the frequency translation. Fast LO devices switching is required to lower frequency conversion losses (ideally equal to $2/\pi$) and commutation noise contributions. Initial simulations have imposed the choice of NPN bipolar transistors for the LO quad. Indeed, the NMOS devices of the BiCMOS technology used do not commutate fast enough to match the 1.8 GHz frequency requirements. The RF differential pair with loads will determinate the main performances of the circuit as indicated by the following equations :

- voltage conversion gain :

$$G_v = (2/\pi)\, G_{mRF}\, Z_L \quad (1)$$

where G_{mRF} is the transconductance of the RF differential pair, Z_L the impedance of the loads.

- RF input voltage dynamic range :

$$V_{dRF} << (I_0/G_{mRF}) \quad (2)$$

- third order intermodulation products :

$$V_{IM3} = \alpha\, Z_L \left(G_{mRF}^3 / I_0^2\right) V_{dRF}^3 \quad (3)$$

where α depends on the RF device.

The requirements impose an RF frequency of 1.8 GHz, an IF output frequency of 110 kHz, and both a conversion gain of +10 dB and an RF power handling of -12 dBm (56 mV_{rms}) at least, leading to an optimization of both intermodulation products, noise level, and power consumption. In the next part, we propose the design of Gilbert mixers featuring either NPN BJT or NMOS devices in their RF input stage.

Design Methodology of Gilbert Mixers

1- Conventional BJT Gilbert mixer

The insertion of emitter degeneration resistors R_E in the RF stage is required to improve the linearity of the BJT differential pair, whose transconductance can then be expressed as follows :

$$G_{mRF} = I_0 / (2U_T + R_E I_0) \quad (4)$$

According to (1) to (4), the performances of the NPN Gilbert mixer are given by the expressions :

$$G_v = (2/\pi)\left[R_L I_0 / (2U_T + R_E I_0)\right] \quad (5)$$

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$$V_{dRF} << 2U_T + R_E I_0 \quad (6)$$

$$V_{IM3} = (2/\pi)\,\alpha_{BJT}\left[R_L I_0 / (2U_T + R_E I_0)^3\right] V_{dRF}^3 \quad (7)$$

where R_L is the impedance of the resistive loads.

Therefore the performances derive from a trade-off between the $R_L.I_0$ and R_E. I_0 products.

The insertion of capacitors on each output branch creates low-pass filters with R_L, removing major unwanted signals from the output spectrum, and thus allowing a lower supply voltage operation. A dedicated DC biasing system has been further developed to impose a good stability of I_0, and the base voltage biasing of the RF and LO devices, with respect to temperature and process drifts that could considerably degrade the performances at low supply voltages. A minimum 2V supply voltage is therefore required to fulfill the +10 dB gain and RF power handling specifications.

DC current I_0 must be optimized regarding both consumption and noise considerations.

The emitter geometry of the LO quad devices has been chosen with respect to fast switching properties and low noise level [2] (i.e. negligible commutation noise contributions). Then, the behavior of the double side band noise figure of the BJT mixer versus I_0 (fig.1) indicate that at low currents, there is a large degradation of the noise figure related to higher R_L and R_E resistors values (i.e. the noise analysis is performed with constant conversion gain and linearity performances). The main noise sources are the thermal noise of R_L and R_E and the shot noise of the collector currents of the BJT RF devices, which is confirmed by the $1/I_0$ noise variations.

For higher I_0 currents, the noise voltage curve deviates from the $1/I_0$ behavior, and tends toward a floor associated with the base resistors of the RF NPN devices. Thus, I_0 is chosen according to the noise figure specification. Then, R_L and R_E are derived to achieve a conversion gain of +10.6 dB and a sufficient input power handling, leading to an IP3 of +5.7 dBm (fig.2). We have designed a mixer featuring 9.8 dB DSB noise figure for a DC current I_0 of 3 mA under a 2 V supply voltage.

The second subsection addresses the design method of a real BiCMOS Gilbert mixer.

2- Real BiCMOS Gilbert mixer

The insertion of NMOS transistors in the RF stage of the mixer potentially offers better linearity than usual NPN BJT devices. The transconductance of the NMOS differential pair is given by the following expression (8) :

$$G_{mRF} = \sqrt{2k(W_{RF}/L_{RF})I_0} = I_0 / (V_{GS\_RF} - V_T) = I_0 / V_{DSat\_RF}$$

where W_{RF} and L_{RF} are the gate width and length of the RF NMOS respectively (L_{RF} is chosen minimum (0.45µm) to perform the 1.8 GHz frequency requirements), V_T is their threshold voltage, and V_{DSat_RF} their drain-to-source saturation voltage.

The ratio W_{RF}/L_{RF} and I_0 will set the trade-off between gain and linearity. The insertion of source degeneration resistors is not required, that is well suited for noise considerations.

Unfortunately, this circuit configuration featuring resistive loads (used in [3]) does not provide a sufficient gain control because of the large dispersion of the threshold voltage of the devices in CMOS processes. To minimize this technology drift, the resistive loads have to be replaced by active loads composed with diode-connected PMOS transistors, whose output impedances are inversely proportional to their transconductance :

$$Z_L = 1/G_{mL} = (V_{GS\_L} - V_T)/I_0 = V_{DSat\_L}/I_0 \quad (9)$$

Therefore the conversion gain becomes :

$$G_v = (2/\pi)(G_{mRF}/G_{mL}) = (2/\pi)(V_{DSat\_L}/V_{DSat\_RF}) \quad (10)$$

where the process and temperature variations are almost completely compensated.

To match the high gain specification, the loads require an important drain-to-source saturation voltage (to lower G_{mL}), and the low supply voltage operation can not be achieved. The final configuration consists in folded diode-connected NMOS loads (fig.3), optimizing the voltage stacking. Then, the performances of the circuit can be expressed as follows :

$$G_v = (2/\pi)(V_{DSat\_L}/V_{DSat\_RF})(I_0/I_L) \quad (11)$$

$$V_{dRF} << (I_L/I_0)\,V_{DSat\_RF} \quad (12)$$

$$V_{IM3} = (2/\pi)\,\alpha_{MOS}\,(I_0/I_L)\left[V_{DSat\_L}/(V_{DSat\_RF})^3\right] V_{dRF}^3 \quad (13)$$

The monitoring of the output current I_L is achieved by the upside current sources. A fraction of I_0 is re-injected into the loads in order to furthermore lower G_{mL} and raise the gain. The drawback of this topology is related to the excessive DC current consumption. The insertion of folded-cascode PMOS transistors featuring high W/L ratios (i.e. low drain-to-source saturation voltages) between the LO stage and the loads, provides a good control of the collector voltage of the LO quad, upside the saturation region. The PMOS devices located in the output paths (folded-cascode and upside current sources), with low cut-off frequencies, act as low-pass filters of the output spectrum, allowing the low supply voltage operation.

The noise analysis derives from the noise behavior of the MOS devices (i.e. the noise of the LO quad is neglected). The main input referred noise sources are :

- the thermal noise of the RF NMOS : $S_{RF}^{th} = \gamma \left(4kT/G_{mRF}\right)$ (14)

- the thermal noise of the NMOS loads : $S_L^{th} = \gamma \left(4kT/G_{mL}\right)\left(1/G_v\right)$ (15)

- the 1/f and thermal noise of the upside PMOS current sources :

$$S_{CS}^{1/f} = \left(1/f\right)\left(\alpha_{CS}/W_{CS}\ L_{CS}\right)\left(\pi/2\right)^2\left(G_{mCS}/G_{mRF}\right)^2 \qquad (16)$$

$$S_{CS}^{th} = \gamma\left(\pi/2\right)^2\left(4kT\right)\left[G_{mCS}/\left(G_{mRF}\right)^2\right] \qquad (17)$$

The RF NMOS and NMOS loads flicker noise components are negligible due to the frequency translation and the large gate length values respectively. Simulations have shown that S_{CS}^{tn} plays a major role on the overall noise level. This source can be minimized by reducing G_{mCS} (i.e. V_{DSat_CS} and W_{CS}/L_{CS}). But the decrease of both V_{DSat_CS} and W_{CS}/L_{CS} is not consistent with output distortion requirements, and the design needs trades-off between low voltage and low noise, low distortion and high gain performances.

The noise analysis of the mixer has been carried out versus I_0 keeping the drain-to-source saturation voltages of the whole MOS constant (i.e. raising the W/L ratios as I_0 increases), in order to maintain conversion gain and linearity values. Figure 4 shows the DSB noise figure versus I_0 for circuits performing +10.6 dB gain and about +6.7 dBm IP3, under a 2.2 V supply voltage. As indicated by equations (14) to (17), the noise figure exhibits a pure $1/I_0$ behavior.

Thus, we have designed a mixer featuring 10.3 dB DSB noise figure for a current I_0 of 3 mA (i.e. a total mixer core DC current ($I_0 + 2I_L$) of 4.7 mA), under a 2.2 V supply voltage. Those results indicate that the BiCMOS structure is well suited for low noise and high linearity applications, and show that our design is among the best ever reported [2] to [7].

Summary

In this paper, we have described an original design methodology of radiofrequency mixers based on Gilbert topologies, providing high performances in term of gain, linearity, noise level and supply voltage. We have presented for the first time a real BiCMOS mixer structure with attractive capabilities. The results indicate that the BiCMOS mixer exhibits greater linearity performances than the conventional BJT one, but worse performances in term of power consumption. This drawback should soon be improved with CMOS technologies featuring lower threshold voltages and 1/f noise levels, and higher cut-off frequencies. The layouts of the circuits are completed, and the results should be presented at the conference.

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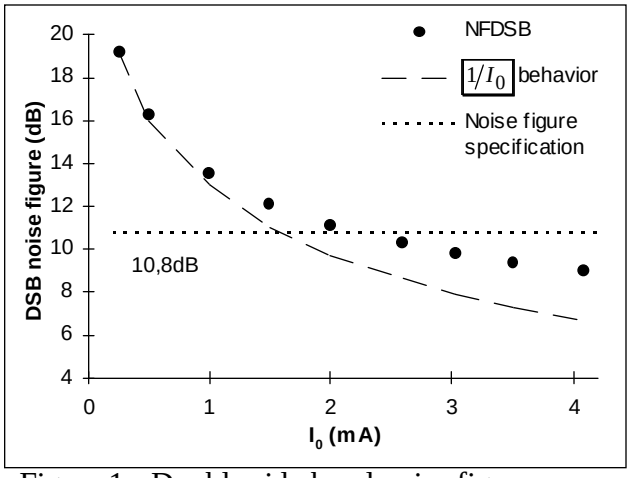

Figure 1 - Double side band noise figure versus I_0 of the conventional BJT Gilbert mixer design

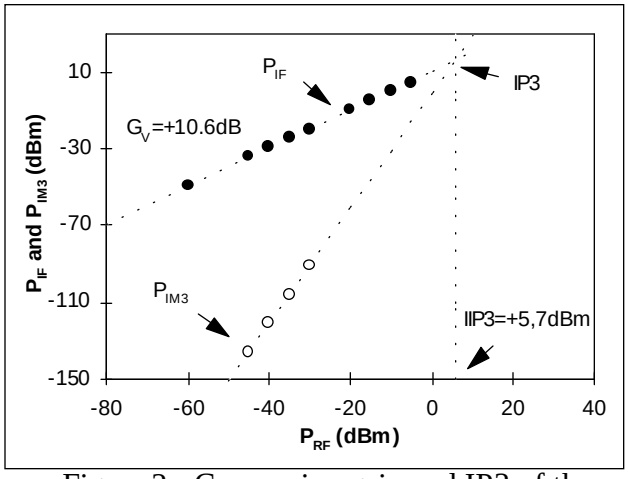

Figure 2 - Conversion gain and IP3 of the conventional BJT Gilbert mixer design

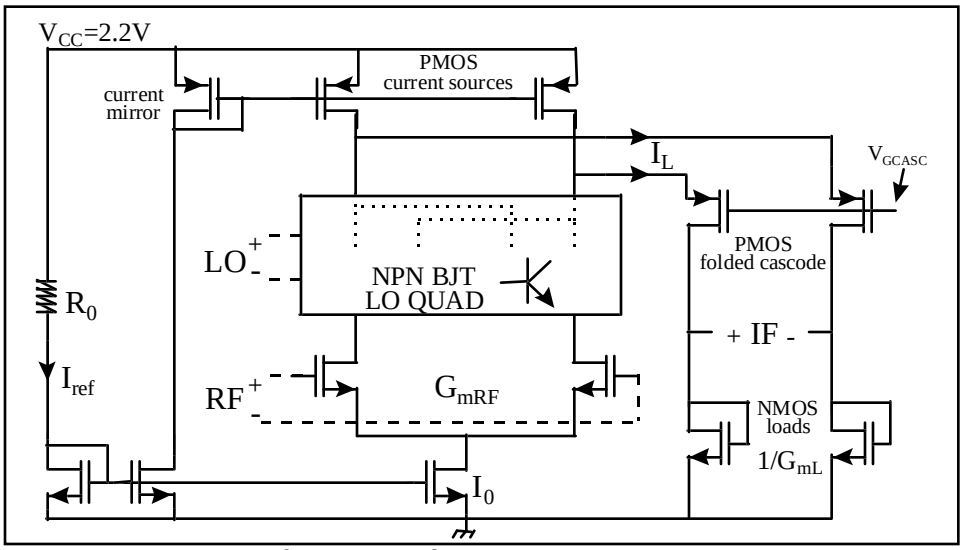

Figure 3 - Final configuration of the real BiCMOS Gilbert mixer design

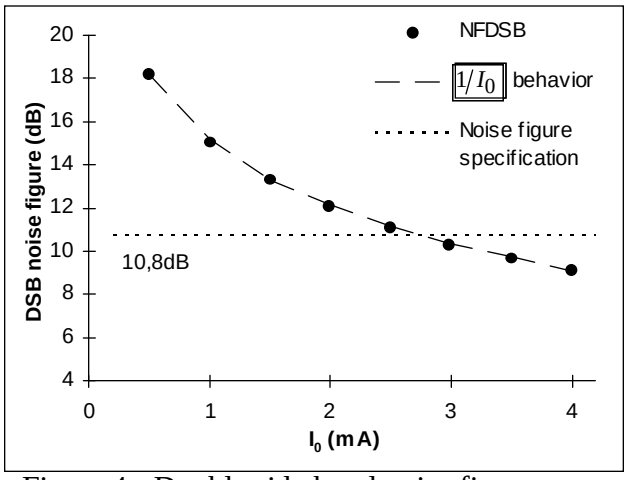

Figure 4 - Double side band noise figure versus I_0 of the real BiCMOS Gilbert mixer design

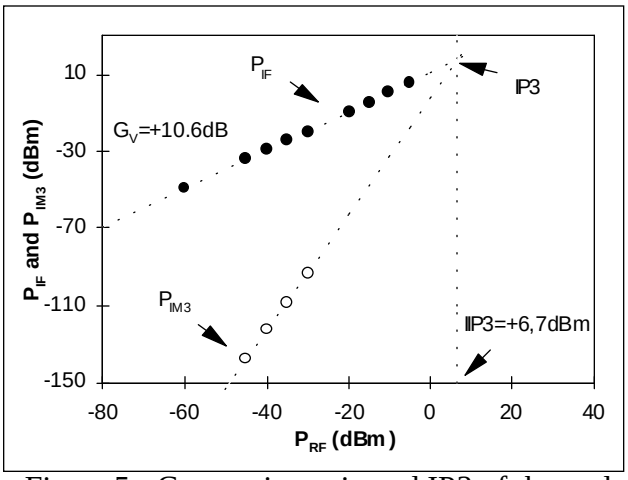

Figure 5 - Conversion gain and IP3 of the real BiCMOS Gilbert mixer design